CLAIMS

1. A method for filling recessed micro-structures at a surface of a semiconductor workpiece with copper metallization comprising the steps of:

depositing a copper layer into the micro-structures with a process generating copper grains that are sufficiently small so as to substantially fill the recessed microstructures;

subjecting the deposited copper to an annealing process at a temperature below about 100 degrees Celsius.

2. A method as claimed in claim 1 wherein the copper is deposited using an electroplating process.

3. A method as claimed in claim 1 wherein an electroplating waveform is used, at least in part, to ensure sufficiently small copper grain size.

4. A method as claimed in claim 1 wherein an electroplating solution additive is used, at least in part, to ensure sufficiently small copper grain size.

5. A method as claimed in claim 1 wherein the annealing process is carried out at ambient room temperature.

6. A method for filling recessed micro-structures at a surface of a semiconductor workpiece with metallization comprising the steps of:

depositing a metal layer into the micro-structures with a process generating copper grains that are sufficiently small so as to substantially fill the recessed microstructures;

subjecting the deposited metal to an annealing process at a temperature below about 100 degrees Celsius.

7. A method as claimed in claim 6 wherein the metal is deposited using an electroplating process.

8. A method as claimed in claim 6 wherein an electroplating waveform is used, at least in part, to ensure sufficiently small metal grain size.

9. A method as claimed in claim 6 wherein an electroplating solution additive is used, at least in part, to ensure sufficiently small metal grain size.

10. A method as claimed in claim 6 wherein the annealing process is carried out at ambient room temperature.

11. A method for filling recessed micro-structures at a surface of a semiconductor workpiece with copper metallization comprising the steps of:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed micro-structures in the at least one dielectric layer;

preparing a surface of the workpiece including the recessed micro-structures with a seed layer for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer to the surface of the wafer to substantially fill the recessed micro-structures;

allowing the electrochemically deposited copper layer to self-anneal for a predetermined period of time at ambient room temperature;

removing copper metallization from the surface of the workpiece except from the recessed micro-structures, said removing step occurring after the predetermined period of time has elapsed.

12. A method as claimed in claim 11 wherein the predetermined period is greater than about 20 hours.

13. A method as claimed in claim 11 wherein the step of preparing a surface of the workpiece comprises:

applying at least one barrier layer over the dielectric layer; and

applying a seed layer over the barrier layer.

14. A method as claimed in claim 13 wherein the step of applying the seed layer is defined by applying the seed layer using a chemical vapor deposition process.

15. A method as claimed in claim 13 wherein the step of applying the seed layer is defined by applying the seed layer using a physical vapor deposition process.

16. A method as claimed in claim 11 wherein the step of preparing a surface of the workpiece comprises:

applying at least one adhesion layer over the dielectric layer; and

applying a seed layer over the adhesion layer.

17. A method as claimed in claim 11 wherein the step of removing the copper metallization is defined by removing the copper metallization using a chemical mechanical polish technique.

18. A method for filling recessed micro-structures at a surface of a semiconductor workpiece with copper metallization comprising the steps of:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed micro-structures in the at least one dielectric layer;

preparing a surface of the workpiece including the recessed micro-structures with a seed layer for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer to the surface of the wafer to substantially fill the recessed micro-structures;

removing copper metallization from the surface of the workpiece except from the recessed micro-structures;

allowing the electrochemically deposited copper layer to self-anneal at ambient room temperature without subjecting the workpiece to a separate and distinct elevated temperature annealing process.

19. A method as claimed in claim 18 wherein the step of preparing a surface of the workpiece comprises:

applying at least one adhesion layer over the dielectric layer; and

applying a seed layer over the adhesion layer.

20. A method as claimed in claim 18 wherein the step of preparing a surface of the workpiece comprises:

applying at least one barrier layer over the dielectric layer; and

applying a seed layer over the barrier layer.

21. A method as claimed in claim 20 wherein the step of applying the seed layer is defined by applying the seed layer using a chemical vapor deposition process.

22. A method as claimed in claim 20 wherein the step of applying the seed layer is defined by applying the seed layer using a physical vapor deposition process.

23. A method as claimed in claim 18 wherein the step of removing the copper metallization is defined by removing the copper metallization using a chemical mechanical polish technique.

24. A method for filling recessed micro-structures at a surface of a semiconductor workpiece with copper metallization comprising the steps of:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed micro-structures in the at least one dielectric layer;

preparing a surface of the workpiece, including the recessed micro-structures, with a seed layer for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer to the surface of the wafer to substantially fill the recessed micro-structures;

subjecting the electrochemically deposited copper layer to an annealing process at a temperature below about 100 degrees Celsius.

25. A method as claimed in claim 24 wherein the step of preparing a surface of the workpiece comprises:

applying at least one adhesion layer over the dielectric layer; and

applying a seed layer over the adhesion layer.

26. A method as claimed in claim 24 wherein the step of preparing a surface of the workpiece comprises:

applying at least one barrier layer over the dielectric layer; and

applying a seed layer over the barrier layer.

27. A method as claimed in claim 26 wherein the step of applying the seed layer is defined by applying the seed layer using a chemical vapor deposition process.

28. A method as claimed in claim 26 wherein the step of applying the seed layer is defined by applying the seed layer using a physical vapor deposition process.

29. A method as claimed in claim 24 wherein the step of removing the copper metallization is defined by removing the copper metallization using a chemical mechanical polish technique.

30. A method for filling recessed micro-structures at a surface of a semiconductor workpiece with copper metallization comprising the steps of:

providing a semiconductor workpiece with a feature that is to be connected with copper metallization;

applying at least one low-K dielectric layer over a surface of the semiconductor workpiece including the feature;

providing recessed micro-structures in the at least one low-K dielectric layer;

preparing a surface of the workpiece, including the recessed micro-structures, with a seed layer for subsequent electrochemical copper deposition;

electrochemically depositing a copper layer to the surface of the wafer to substantially fill the recessed micro-structures;

subjecting the electrochemically deposited copper layer to an annealing process at a temperature below which the low-K dielectric layer substantially degrades.

31. A method as claimed in claim 30 wherein the annealing step takes place at a temperature corresponding to a baking temperature of the low-K dielectric.